

# Exhibit 5

# **Exhibit A**

**U.S. Pat. No. 9,218,156**  
**Claim 7**

**'156 PATENT****7. A device comprising:**

at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,

wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least  $X=5\%$  of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least  $X\%$  of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least  $Y=0.05\%$  from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

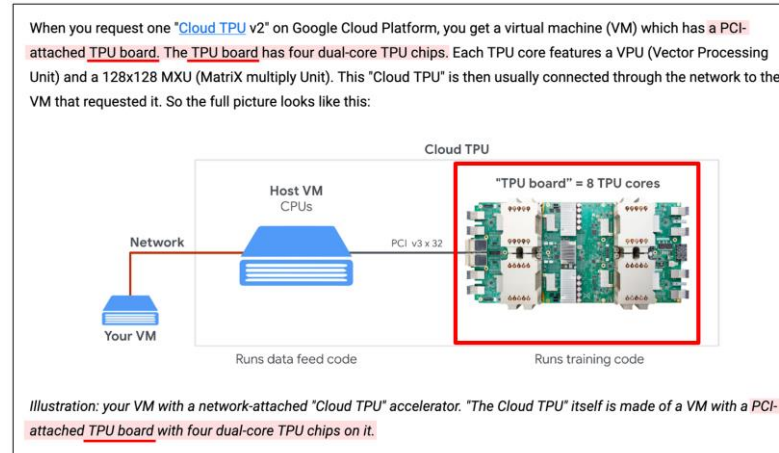
at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit

wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

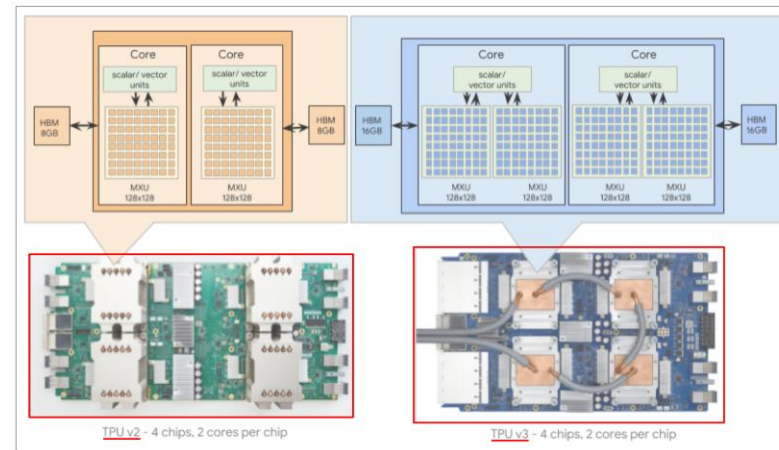
wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

**INFRINGEMENT EVIDENCE**

As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed "device." For example, a "TPU Board" satisfies these requirements:



<https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2><sup>1</sup>



<https://cloud.google.com/tpu/docs/system-architecture>

<sup>1</sup> Unless indicated otherwise, color-coded annotations have been added in order to identify relevant components and features of the Accused Products.

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7. A **device** comprising:

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wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least  $X=5\%$  of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least  $X\%$  of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least  $Y=0.05\%$  from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit

wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

## INFRINGEMENT EVIDENCE

As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed "device." For example, a "TPU Chip" satisfies these requirements:

When you request one "Cloud TPU v2" on Google Cloud Platform, you get a virtual machine (VM) which has a PCI-attached TPU board. The TPU board has four dual-core TPU chips. Each TPU core features a VPU (Vector Processing Unit) and a 128x128 MXU (Matrix multiply Unit). This "Cloud TPU" is then usually connected through the network to the VM that requested it. So the full picture looks like this:

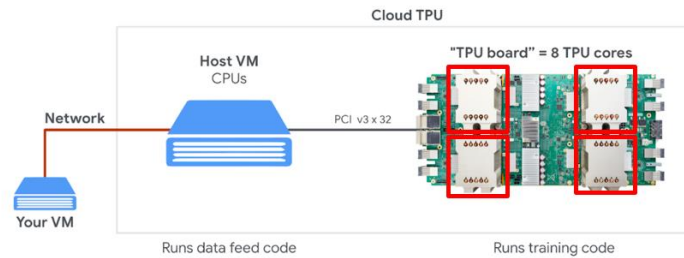
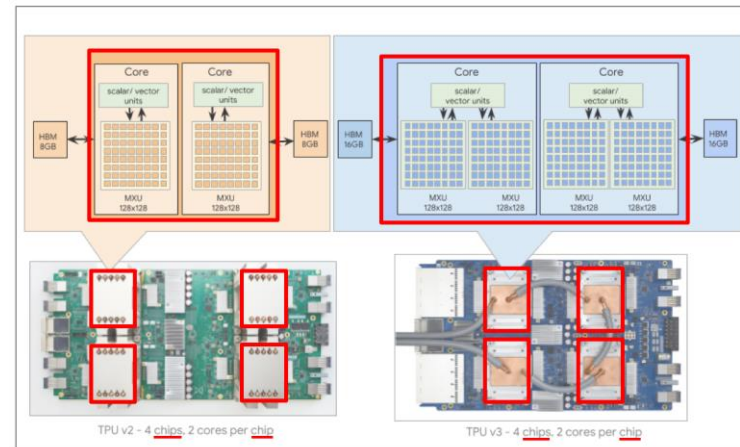


Illustration: your VM with a network-attached "Cloud TPU" accelerator. "The Cloud TPU" itself is made of a VM with a PCI-attached TPU board with four dual-core TPU chips on it.

<https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2>



<https://cloud.google.com/tpu/docs/system-architecture>

See also generally Norrie et al., "Google's Training Chips Revealed: TPuv2 and TPuv3" (Presented at HotChips Conference, Aug. 2020)

<sup>2</sup> Unless indicated otherwise, color-coded annotations have been added to the figures in this chart to highlight relevant teachings of the prior art.

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at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit

wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

## INFRINGEMENT EVIDENCE

As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed "device." For example, a "TPU Core" satisfies these requirements:

When you request one "Cloud TPU v2" on Google Cloud Platform, you get a virtual machine (VM) which has a PCI-attached TPU board. The TPU board has four dual-core TPU chips. Each TPU core features a VPU (Vector Processing Unit) and a 128x128 MXU (Matrix multiply Unit). This "Cloud TPU" is then usually connected through the network to the VM that requested it. So the full picture looks like this:

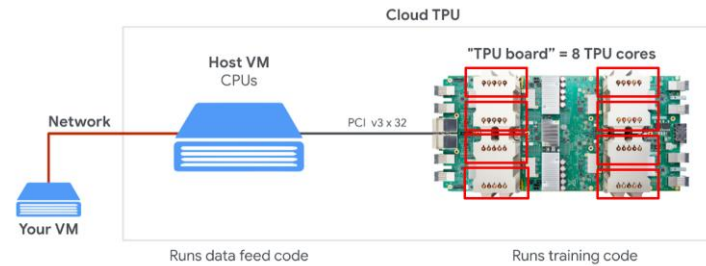
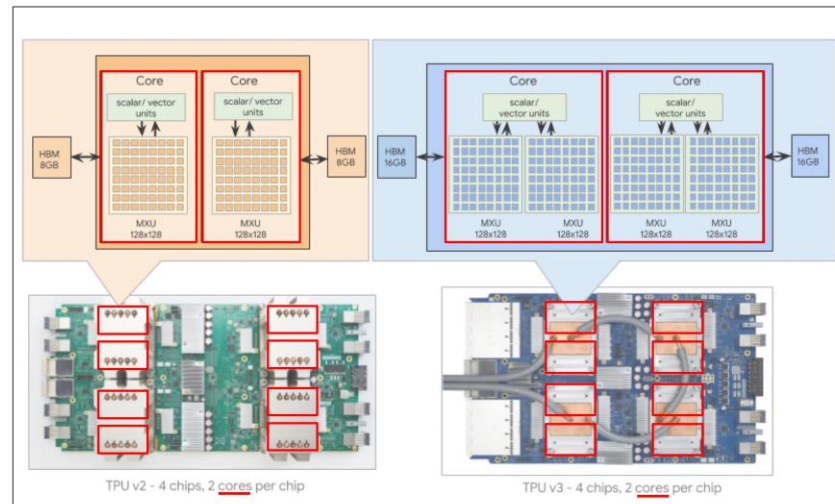


Illustration: your VM with a network-attached "Cloud TPU" accelerator. "The Cloud TPU" itself is made of a VM with a PCI-attached TPU board with four dual-core TPU chips on it.

<https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2>



<https://cloud.google.com/tpu/docs/system-architecture>



## '156 PATENT

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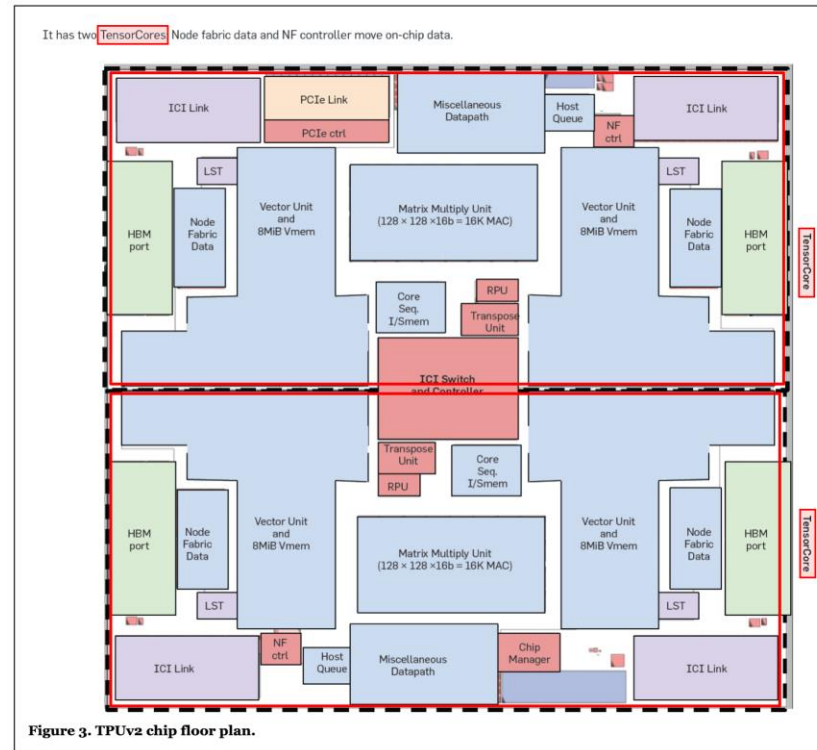
wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least  $X=5\%$  of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least  $X\%$  of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least  $Y=0.05\%$  from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit

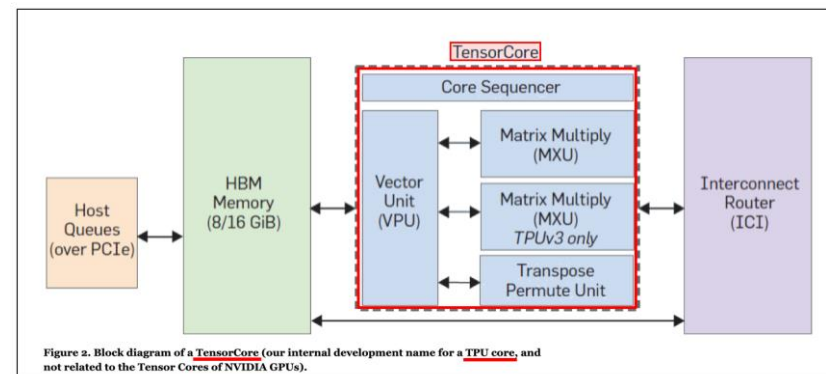
wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

## INFRINGEMENT EVIDENCE



<https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks>



*Id.*

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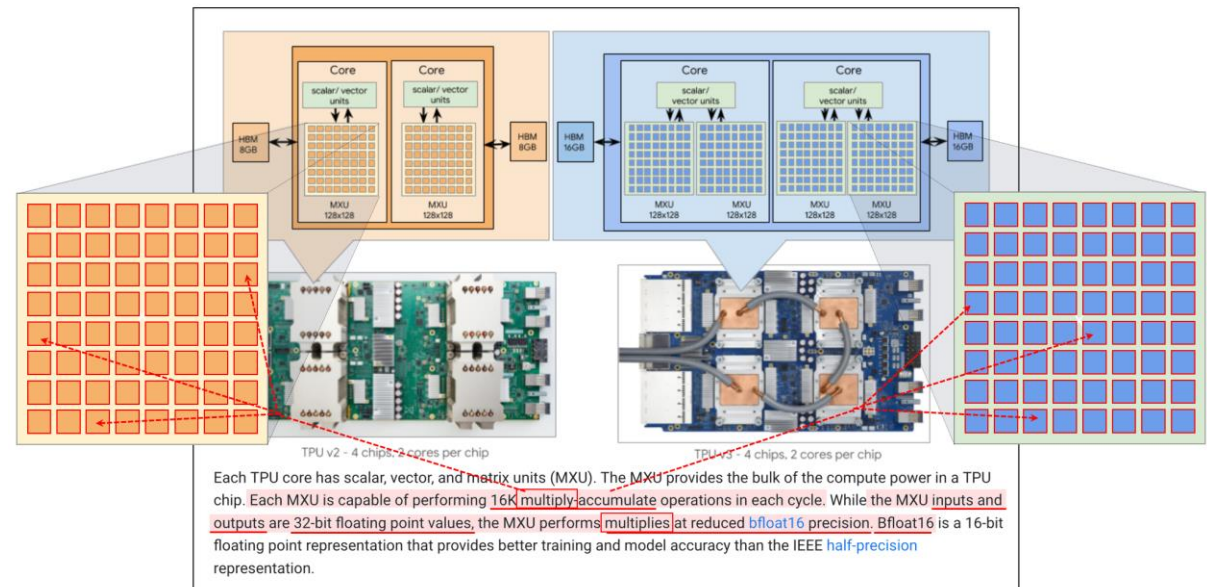
wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from  $1/1,000,000$  through  $1,000,000$  and for at least  $X=5\%$  of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least  $X\%$  of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least  $Y=0.05\%$  from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

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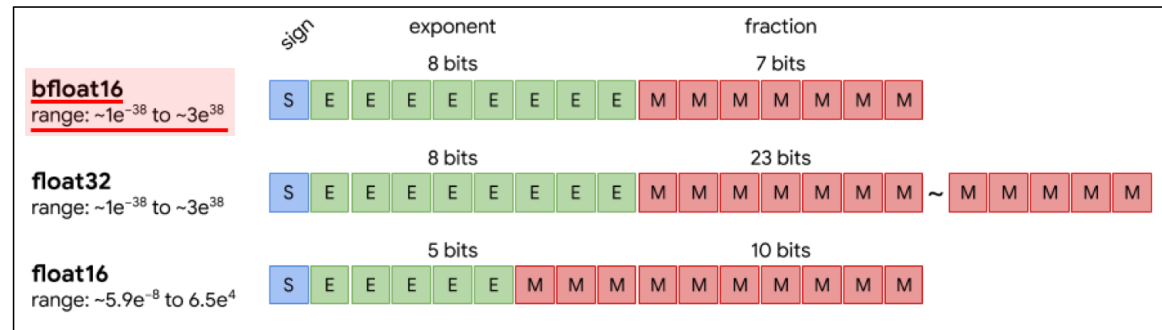
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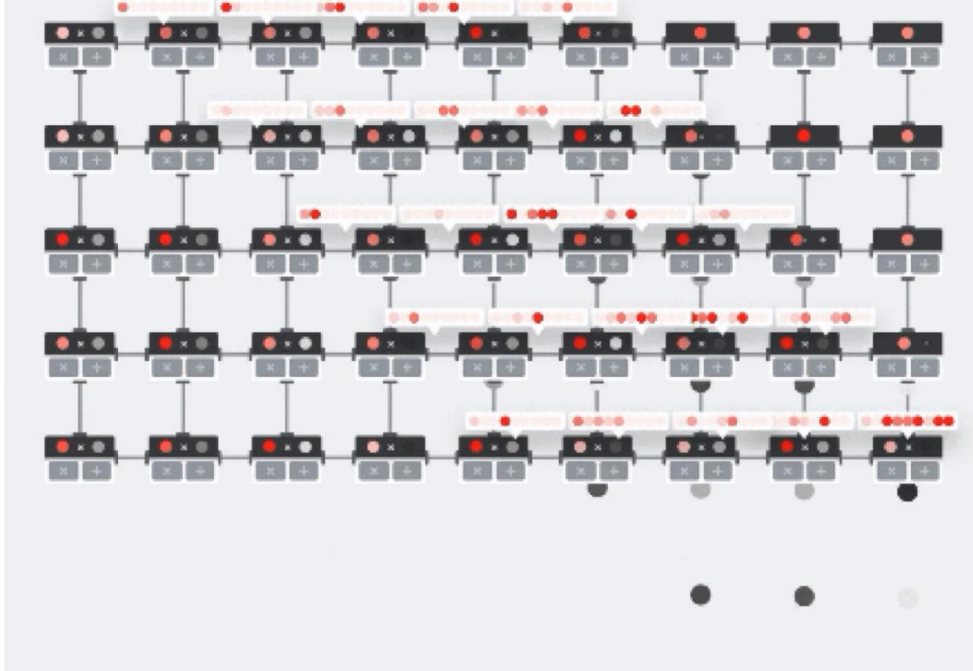
## INFRINGEMENT EVIDENCE



<https://cloud.google.com/tpu/docs/system-architecture>

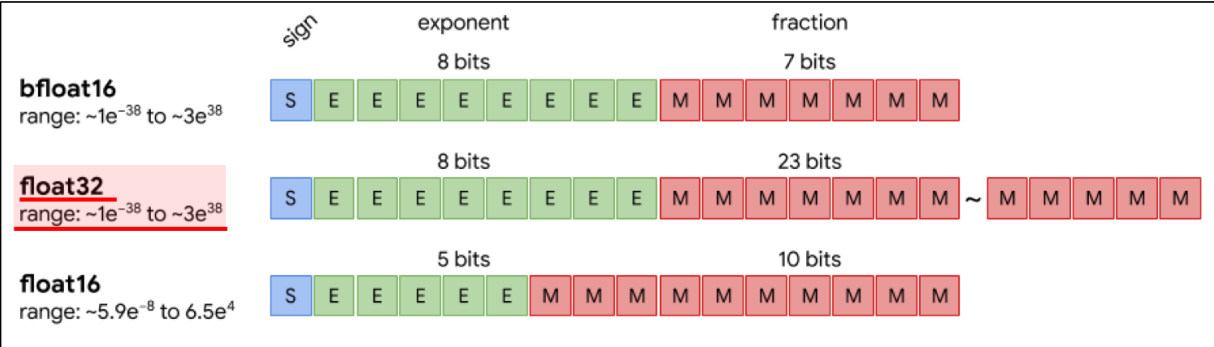


<https://cloud.google.com/tpu/docs/bfloat16>

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<p>7. A device comprising:</p> <p><b>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</b></p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<p><b>Systolic array</b></p> <p>The MXU implements matrix multiplications in hardware using a so-called "systolic array" architecture in which <u>data elements flow through an array of hardware computation units.</u> (In medicine, "systolic" refers to heart contractions and blood flow, here to the flow of data.)</p> <p>The basic element of a matrix multiplication is a dot product between a line from one matrix and a column from the other matrix (see illustration at the top of this section). For a matrix multiplication <math>Y=X*W</math>, one element of the result would be:</p> $Y[2,0] = X[2,0]*W[0,0] + X[2,1]*W[1,0] + X[2,2]*W[2,0] + \dots + X[2,n]*W[n,0]$  <p><i>Illustration: the MXU systolic array. The compute elements are multiply-accumulators. <u>The values of one matrix are loaded into the array (red dots).</u> <u>Values of the other matrix flow through the array (grey dots).</u> Vertical lines propagate the values up. Horizontal lines propagate partial sums. It is left as an exercise to the user to verify that as the data flows through the array, you get the result of the matrix multiplication coming out of the right side.</i></p> <p><a href="https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2">https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2</a></p>



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<p>7. A device comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p><b>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</b></p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<ul style="list-style-type: none"> <li>• “<b>Each of the cores on a TPU device can execute user computations (XLA ops)</b> independently.” <a href="https://cloud.google.com/tpu/docs/system-architecture#pod">https://cloud.google.com/tpu/docs/system-architecture#pod</a></li> <li>• “<b>TPUs use a VLIW architecture to express instruction-level parallelism to the many compute units of a TensorCore. XLA uses standard VLIW compilation techniques</b> including loop unrolling, instruction scheduling, and software pipelining to keep all compute units busy and to simultaneously move data through the memory hierarchy to feed them.” <a href="https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext">https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext</a></li> <li>• “The <b>Core Sequencer</b> fetches VLIW (Very Long Instruction Word) instructions from the core's on-chip, software-managed Instruction Memory (Imem), executes scalar operations using a 4K 32-bit scalar data memory (Smem) and 32 32-bit scalar registers (Sregs), and forwards vector instructions to the VPU. <b>The 322-bit VLIW instruction can launch eight operations: two scalar, two vector ALU, vector load and store, and a pair of slots that queue data to and from the matrix multiply and transpose units. The XLA compiler schedules loading Imem via independent overlays of code, as unlike conventional CPUs, there is no instruction cache.</b>” <i>Id.</i></li> <li>• “The <b>Vector Processing Unit (VPU)</b> performs vector operations using a large on-chip vector memory (Vmem) with 32K 128 x 32-bit elements (16MiB), and 32 2D vector registers (Vregs) that each contain 128 x 8 32-bit elements (4 KiB). <b>The VPU streams data to and from the MXU through decoupling FIFOs. The VPU collects and distributes data to Vmem via data-level parallelism (2D matrix and vector functional units) and instruction-level parallelism (8 operations per instruction).</b>” <i>Id.</i></li> </ul> <div data-bbox="919 821 1776 1218"> <p>Figure 2. Block diagram of a TensorCore (our internal development name for a TPU core, and not related to the Tensor Cores of NVIDIA GPUs).</p> </div> <p><i>Id.</i></p>

'156 PATENT	INFRINGEMENT EVIDENCE
<p>7. A device comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;</p> <p><b>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine;</b> and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<ul style="list-style-type: none"> <li>• “The <b>Core Sequencer</b> fetches <b>VLIW (Very Long Instruction Word)</b> instructions from the core's on-chip, software-managed <b>Instruction Memory (Imem)</b>, executes scalar operations using a <b>4K 32-bit scalar data memory (Smem)</b> and <b>32 32-bit scalar registers (Sregs)</b>, and forwards vector instructions to the VPU. The 322-bit VLIW instruction can launch eight operations: two scalar, two vector ALU, vector load and store, and a pair of slots that queue data to and from the matrix multiply and transpose units. The XLA compiler schedules loading Imem via independent overlays of code, as unlike conventional CPUs, there is no instruction cache.”</li> </ul> <p><i>Id.</i></p> <ul style="list-style-type: none"> <li>• “The <b>Vector Processing Unit (VPU)</b> performs vector operations using a large on-chip <i>vector memory (Vmem)</i> with 32K 128 x 32-bit elements (16MiB), and 32 2D <i>vector registers (Vregs)</i> that each contain 128 x 8 32-bit elements (4 KiB). <b>The VPU streams data to and from the MXU through decoupling FIFOs. The VPU collects and distributes data to Vmem via data-level parallelism (2D matrix and vector functional units) and instruction-level parallelism (8 operations per instruction).</b>”</li> </ul> <p><i>Id.</i></p> <div data-bbox="852 586 1839 1040"> <p>Figure 2. Block diagram of a TensorCore (our internal development name for a TPU core, and not related to the Tensor Cores of NVIDIA GPUs).</p> </div> <p><i>Id.</i></p> <ul style="list-style-type: none"> <li>• “<b>Each of the cores on a TPU device can execute user computations (XLA ops)</b> independently.”  <a href="https://cloud.google.com/tpu/docs/system-architecture#pod">https://cloud.google.com/tpu/docs/system-architecture#pod</a></li> <li>• “<b>TPUs use a VLIW architecture to express instruction-level parallelism to the many compute units of a TensorCore. XLA uses standard VLIW compilation techniques</b> including loop unrolling, instruction scheduling, and software pipelining to keep all compute units busy and to simultaneously move data through the memory hierarchy to feed them.”  <a href="https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext">https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext</a></li> </ul>

**'156 PATENT****7. A device comprising:**

at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,

wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least  $X=5\%$  of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least  $X\%$  of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least  $Y=0.05\%$  from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;

wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

**INFRINGEMENT EVIDENCE**

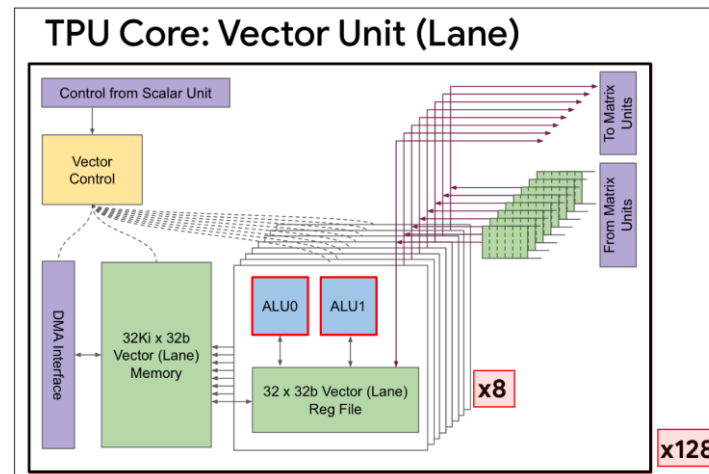
The Accused Products independently meet this claim limitation for each “device” identified above:

We cannot reveal technology details of our chip partner. Although it is in a larger, older technology, the TPUv2 die size is less than 3/4s of the GPU. TPUv3 is 6% larger in that same technology. TDP stands for Thermal Design Power. The Volta has 80 symmetric multiprocessors.

Feature	TPUv1	TPUv2	TPUv3	Volta
Peak TeraFLOPS/Chip	92 (8b int)	46 (16b) 3 (32b)	123 (16b) 4 (32b)	125 (16b) 16 (32b)
Network links x Gbits/s/Chip	—	4 x 496	4 x 656	6 x 200
Max chips/supercomputer	—	256	1024	Varies
Peak PetaFLOPS/supercomputer	—	11.8	126	Varies
Bisection Terabits/supercomputer	—	15.9	42.0	Varies
Clock Rate (MHz)	700	700	940	1530
TDP (Watts)/Chip	75	280	450	450
TDP (Kwatts)/supercomputer	—	124	594	Varies
Die Size (mm <sup>2</sup> )	<331	<611	<648	815
Chip Technology	28nm	>12nm	>12nm	12nm
Memory size (on/off-chip)	28MB/8GB	32MB/16GB	32MB/32GB	36MB/32GB
Memory GB/s/Chip	34	700	800	900
MXUs/Core	1	1	2	8
MXU Size	256x256	128x128	128x128	4x4
Cores/Chip	1	2	2	80
Chips/CPU Host	4	4	8	8 or 16

**Table 3. Key processor features.**

<https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext>



Norrie et al., “Google’s Training Chips Revealed: TPUv2 and TPUv3”  
(Presented at HotChips Conference, Aug. 2020)